RTCSA 2017 Program

Time	August 16		Time	August 17	Time	August 18	
08:00-08:45	Registration						
			08:30-09:00	Registration	08:30-09:00	Registration	
8:45-10:00	RTCSA Opening Remark & Keynote (100)						
			09:00-10:00	RTCSA/NVMSA Joint Keynote (100)	09:00-10:00	RTCSA/NVMSA Joint Keynote (100)	
10:00-10:30	Coffee Break		10:00-10:30	Coffee Break	10:00-10:30	Coffee Break	
10:30-12:00	Session 1 (106)	Invited1 (101)	10:30-12:00	Panel Discussion (100)	10:30-12:00	Session 4 (106)	Session 5 (101)
12:00-13:30	Lunch		12:00-13:30	Lunch	12:00-13:30	Lunch	
13:30-15:00	Session 2 (106)	Short1 (101)	13:30-18:00	Local Tour	13:30-15:00	Session 6 (106)	Short2 (101)
15:00-15:30	Coffee Break				15:00-	Conference Closing	
15:30-17:30	Session 3 (106)	Invited2 (101)					
17:30-18:00							
18:00-21:00	Welcome Reception & Poster Session (Landis Inn Chuhu)		18:00-21:00	Conference Banquet & Best Paper Award (Landis Inn Chuhu)			

Conference Venue: Microelectronics and Information Systems Research Center

100: International Conference Hall

101: Conference Room 1

106: Conference Room 4

Welcome Reception and Conference Banquet: Landis Inn Chuhu

RTCSA Keynote (August 16): Prof. Sandeep K. Shukla

Room: International Conference Hall (100)

Title: *Cyber Security of Cyber Physical Critical Infrastructures: A Case for a Schizoid Design Approach*

Abstract:

In the past, the design of cyber physical systems (CPS) required a model based engineering approach -- a design methodology consisting of physics based mathematical modeling of the physical system, and a control theoretic modeling of the control system put together in a formal or semi-formal framework. The designers would start from an abstract model, and refine it down to an implementation model in several steps, either formally or informally. The implementation model is then validated for functional correctness, and satisfaction of performance, real-time schedulability goals. Functional Safety, robustness to input assumptions, reliability under fault assumptions, and resilience to unknown adversities were considered as important design goals for safety-critical CPS. With the increased use of networked distributed control of large and geographically distributed critical infrastructures such as smart grid and the exposure to cyber-attacks ushered in by the IP-convergence phenomenon -- designers must now consider cyber-security and cyber defense as first class design objectives. However, in order to do so, designers have to don a dual personality -- while designing for robustness, reliability, functional safety -- a model driven engineering approach would work -- for designing for cyber-security and defense, the designer has to enter the mindset of a malicious attacker. For instance, one has to consider the various observations or sampling points of the system (e.g. sensors to read or sample the physical environment), and think how an attacker might compromise the unobservability of those points without authentication, and what knowledge of the system dynamics or the control mechanism of the system might be actually reconstructed by the attacker. One also has to consider the actuation points of the system, and ponder the least number of such actuation points the attacker has to take over in order to disrupt the dynamics of the system enough to create considerable damage. One must envision how to obfuscate the dynamics of the system even when certain sensing or actuation points are compromised. Also, it is known that a large percentage of attacks are induced by insider or a collusion of internal and external agents. Thus, perimeter defense alone cannot defend the system. In such cases, the symptoms of an ongoing attack in the dynamics of the system itself must be discerned continually. This approach to viewing the system from an adversarial position requires us to topple the design paradigm over its head, and we will need to build models from data, and not just generate data from models. The designer must observe a system in action – even through partial observations, and construct a model close enough to the real system model – and then use the partial access to create damages to the because the approximate model allows her to do so. Almost like a schizophrenic duality, the engineer also has to wear the designers hat, and consider a game in which the observations are obfuscated enough to render it impossible for an attacker to build any useful model to induce clever attacks. The designer has to worry if she can construct from unobfuscated observations, a dynamics quickly enough so that the difference between the expected dynamics and the real dynamics can trigger alarms to alert the system administrators. In this talk, while discussing this view of system design, we will also talk about VSCADA -- a virtual distributed SCADA lab we created for

modeling SCADA systems for critical infrastructures, and how to use such a virtual lab completely implemented in simulation -- to achieve the cyber security and cyber defense objectives of critical infrastructures -- through attack injections, attack detection, and experiments on new defense mechanisms. We will also discuss the real SCADA test bed we are building at our center for cyber security of critical infrastructures at IIT Kanpur.

Biography:

Professor Sandeep K. Shukla is an IEEE fellow, an ACM Distinguished Scientist, and serves as an IEEE Computer Society Distinguished Visitor, and as an ACM Distinguished Speaker. He is currently the Editor-in-Chief of ACM Transactions on Embedded Systems, and associate editor for ACM transactions on Cyber Physical Systems. In the past, he has been associate editors for IEEE Transactions on Computers, IEEE Transactions on Industrial Informatics, IEEE Design & Test, IEEE Embedded Systems Letters, and many other journals. He has guest-edited more than 15 special issues for various IEEE and ACM journals. He has written or edited 9 books, published over 200 journal and conference papers. He has been program chairs for 4 IEEE/ACM International conferences, and General Chair for 2 of these conferences. He has served on the program committee of more than 100 international conferences and workshops. He supervised 12 PhDs, and directed five post-doctoral scholars at Virginia Tech. Sandeep's current research focus is on Cyber Security for Critical Infrastructures. He is coordinating a research center on cyber security for critical infrastructures along with his colleagues at IIT Kanpur now.

He received his bachelor's degree in Computer Science and Engineering at Jadavpur University, Kolkata in 1991, his Masters and PhD degrees in Computer Science from the State University of New York at Albany, NY, USA in 1995 and 1997 respectively. He worked as a scientist at the GTE labs on telecommunications network management, distributed object technology, and event correlation technologies between 1997 and 1999. Between 1999 and 2001, he worked at the Intel Corporation on the formal verification of the ITANIUM processor, and on system level design languages. 2001-2002, he was a research faculty at the University of California at Irvine working on embedded system design. From 2002 till 2015, he has been an assistant, associate, and full professor at Virginia Tech, USA. He co-founded the Center for Embedded Systems for Critical Applications (CESCA) in 2007, and has been a director of the center between 2010 and 2012. In 2015, he joined the Computer Science and Engineering Department of the Indian Institute of Technology Kanpur, India. He is currently the department head of Computer Science & Engineering, Poonam and Prabhu Goel Chair Professor, and Dr.Deep Singh and Daljeet Kaur Faculty Fellow at IIT Kanpur. He received the Ramanujan Fellowship from the Science and Engineering Research Board, Government of India, the Presidential Early Career Award for Scientists and Engineers (PECASE) from the White House in 2004, Frederich Wilhelm Bessel Award in 2008 from the Humboldt Foundation, Germany, Virginia Tech Faculty Fellow Award, A distinguished Alumni Award from the State University of New York at Albany, A best paper award at the Asia-Pacific Design Automation Conference, GTE Laboratories Excellence Award,ASEE/ONR Faculty Fellowship in 2005, ASEE/Air Force Senior Faculty Fellowship in 2007, and an Air Force Labs Faculty Fellowship in 2008. Sandeep also has been a visiting faculty at INRIA, France, University of Kaiserslautern in Germany, MIT, and University of Birmingham UK for various periods of time.

RTCSA/NVMSA Joint Keynote (August 17): Prof. Cheng-Wen Wu

Room: International Conference Hall (100)

Title: *Will AI and IOT Make Semiconductor Memories Great Again?*

Abstract:

The global semiconductor business over the past thirty years shows an encouraging trend of growth in general, with only a few glitches that did not hinder the long-term trend. The growing trend, however, slows down in recent years with the saturating smartphone market, until late 2016 when AI suddenly gave everybody new hope. Meanwhile, the Internet-of-Things (IOT) has long been identified, or expected, as the main driving force of growth for many industries in the future. Unfortunately, so far IOT is not giving a great boost to the semiconductor industry, due to limitations in global economy and energy consumption. What, then, are the specific problems and challenges to semiconductors? If IOT is going to give a boost to the stagnant semiconductor industry, what will be the key factors of its success? Is it AI? In my speech, I will try to address these issues, and propose the Symbiotic System Model (SSM) for developing IOT devices and systems. I will also give my observations on the role of semiconductor memories in the AI/IOT era. This speech is meant for triggering more research activities regarding establishing a sound IOT platform that allows heterogeneous integration of technologies and partners to migrate certain industries based on the notion of IOT.

Biography:

Cheng-Wen Wu received the BSEE degree from National Taiwan University in 1981, and the MS and PhD degrees in ECE from UCSB in 1985 and 1987, respectively. Since 1988, he has been with the Department of EE, National Tsing Hua University (NTHU), Hsinchu, Taiwan, where he is currently a Tsing Hua Distinguished Chair Professor. He has served in the past at NTHU as the Director of Computer Center, Chair of EE Department, Director of IC Design Technology Center, Dean of the College of EECS, and Senior Vice President for Research. When he was on leave from NTHU from 2007 to 2014, he served at ITRI as the General Director of the SOC Technology Center, and the Vice President and General Director of the Information and Communications Labs. Dr. Wu received the Distinguished Teaching Awards (twice) from NTHU, the Outstanding Electrical Engineering Professor Award from the Chinese Institute of Electrical Engineers (CIEE), the Distinguished Research Awards (three times) from National Science Council, the Industrial Collaboration Awards (twice) from the Ministry of Education (MOE), the Academic Award from the Ministry of Education (MOE), the National Endowed Chair Professorship from MOE, the EE Medal (highest honor) from CIEE, etc. His current research interests include test and repair of semiconductor memories, and design and test of symbiotic IOT devices and systems. He is a life member of the CIEE, a life member of Taiwan IC Design Society, a Fellow of the ROC Technology Management Society, and a Fellow of the IEEE.

RTCSA/NVMSA Joint Keynote (August 18): Prof. David H.C. Du

Room: International Conference Hall (100)

Title: *Can Emerging Non-Volatile Memory Help Solving Big Data Problems?*

Abstract:

The emerging Non-Volatile Memory (NVRAM) has recently generated quite a bit excitements. Due to its non-volatile property, it can be used as either main memory or storage. Flash memory-based solid state drives (SSD) have already replaced high performance hard disk drives (HDD). Other types of NVRAM like PCM, MRAM, and STT-RAM have the potential to replace DRAM as main memory. At the meantime, our computing and communication environment has dramatically changed by the huge amount data been generated and processed daily. We intend to fully utilize the collected data for making critical decisions to benefit individuals, business, and society (big data problems). Therefore, we like to ask the following questions. Can emerging NVRAM help solving big data problems? With the boundary of memory and storage becoming blurred, what are to be changed in computer architecture, operating systems and software/applications? How do we deal with special properties of NVRAM including read/write asymmetric performance, endurance problem, and data consistent issue?

Biography:

David H.C. Du (杜宏章) – received the B.S. degree in mathematics from National Tsing-Hua University, Taiwan, R.O.C. in 1974, and the M.S. and Ph.D. degrees in computer science from the University of Washington, Seattle, in 1980 and 1981, respectively.

He is currently the Qwest Chair Professor at the Computer Science and Engineering Department, University of Minnesota, Minneapolis and the Director of NSF I/UCRC Center Research on Intelligent Storage. He is also an IEEE Fellow and a Fellow of Minnesota Supercomputing Institute. He has served as a member of Advisory Committee of IIS and CITI in Academic Sinica, III and ITRI in Taiwan. His research interests include cyber security, sensor networks, multimedia computing, storage systems, high-speed networking, high-performance computing, database design and CAD for VLSI circuits. He has authored and co-authored more than 280 technical papers, including 120 referred journal publications in his research areas. He has also graduated 60 Ph.D. and 100+ M.S. students. Dr. Du is an IEEE Fellow and a Fellow of Minnesota Supercomputer Institute. He is currently served on a number of journal editorial boards. He has also served as guest editors for a number of journals including IEEE Computer, IEEE and Communications of ACM. He has also served as Conference Chair and Program Committee Chair to several major conferences in multimedia, database, security and networking areas.

Invited Session 1: Flexible and Reliable Models in Cyber-Physical Systems

Session Chair: Prof. Jian-Jia Chen

Room: Conference Room 1 (101)

300	10:30-11:00	State of the Art for Scheduling and Analyzing Self-Suspending Sporadic Real-Time Tasks
		Jian-Jia Chen, Georg von der Br¨uggen, Wen-Hung Huang, and Cong Liu
301	11:00-11:30	Benchmarking OpenMP Programs for Real-Time Scheduling
		Yang Wang, Nan Guan, Jinghao Sun, Mingsong Lv, Qingqiang He, Tianzhang He, Wang Yi1
302	11:30-12:00	A Generic Framework Facilitating Early Analysis of Data Propagation Delays in Multi-Rate Systems

		Matthias Becker, Saad Mubeen, Dakshina Dasari, Moris Behnam, and Thomas Nolte
Invited Session 2: Non-Volatile Processor **Session Chair: Prof. Chun Jason Xue** **Room: Conference Room 1 (101)**		
200	15:30-16:00	Distillation: A Light-Weight Data Separation Design to Boost Performance of NVDIMM Main Memory
		Che-Wei Tsao, Yuan-Hao Chang, Tei-Wei Kuo, and Shau-Yin Tseng
201	16:00-16:30	Maximize Energy Utilization for Ultra-Low Energy Harvesting Powered Embedded Systems
		Chen Pan, Mimi Xie, and Jingtong Hu
202	16:30-17:00	Retention State-Enabled and Progress-Driven Energy Management for Self-powered Non-volatile Processors
		Zhiyao Gong, Keni Qiu, Dongqin Zhou, Weiwen Chen, Yuanchao Xu, Xin Shi and Yongpan Liu
203	17:00-17:30	Energy-aware Morphable Cache Management for Self-powered Non-volatile Processors
		Yang Zhou, Mengying Zhao, Lei Ju, Chun Jason Xue, Xin Li, Zhiping Jia

Session 1: Designs for mobile devices and networked systems **Session Chair: Prof. Jingtong Hu** **Room: Conference Room 4 (106)**		
28	10:30-11:00	Effectively Utilizing Elastic Resources in Networked Control Systems
		Michael Balszun, Debayan Roy, Licong Zhang, Wanli Chang, and Samarjit Chakraborty
47	11:00-11:30	An Empirical Study of F2FS on Mobile Devices
		Yu Liang, Chenchen Fu, Yajuan Du, Aosong Deng, Mengying Zhao, Liang Shi, and Chun Jason Xue
53	11:30-12:00	A Reliable MAC for Delay-Bounded and Energy-Efficient WSNs
		Philip Parsch and Alejandro Masrur
Session 2: Towards IoT and CPS **Session Chair: Prof. Eduardo Tovar** **Room: Conference Room 4 (106)**		
3	13:30-14:00	A Configurable Synchronous Intersection Protocol for Self-Driving Vehicles
		Shunsuke Aoki and Raj Rajkumar
14	14:00-14:30	Real-Time Dense Wired Sensor Network Based on Traffic Shaping
		João Loureiro, Raghuraman Rangarajan, Borislav Nicolic, Leandro Indrusiak, and Eduardo Tovar
48	14:30-15:00	Exploiting Space Buffers for Emergency Braking in Highly Efficient Platoons
		Dharshan Krishna Murthy, and Alejandro Masrur

Session 3: GPUs and resource sharing **Session Chair: TBD** **Room: Conference Room 4 (106)**		
57	15:30-16:00	A Server-based Approach for Predictable GPU Access Control
		Hyoseung Kim, Pratyush Patel, Shige Wang, and Raj Rajkumar
20	16:00-16:30	Worst-Case Execution Time Analysis of GPU Kernels
		Yijie Huangfu and Wei Zhang
40	16:30-17:00	An Optimal Spin-Lock Priority Assignment Algorithm for Real-Time Multi-core Systems
		Sara Afshar, Moris Behnam, Reinder J. Bril, and Thomas Nolte
6	17:00-17:30	New Schedulability Analysis for MrsP
		Shuai Zhao, Jorge Garrido, Alan Burns, and Andy Wellings
Session 4: Multiprocessors and multicore processors **Session Chair: TBD** **Room: Conference Room 4 (106)**		
22	10:30-11:00	Fixed-Priority Scheduling of Mixed Soft and Hard Real-Time Tasks on Multiprocessors
		Jian-Jia Chen, Wen-Hung Huang, Zheng Dong, and Cong Liu
56	11:00-11:30	Schedulability Analysis for Global Fixed-Priority Scheduling of the 3-Phase Task Model
		Cláudio Maia, Geoffrey Nelissen, Luís Nogueira, Luis Miguel Pinho, and Daniel Gracia Pérez
49	11:30-12:00	A Scheduling Framework for Handling Integrated Modular Avionic Systems on Multicore Platforms
		Alessandra Melani, Renato Mancuso, Marco Caccamo, Giorgio Buttazzo, Johannes Freitag, and Sascha Uhrig
Session 5: Scheduling and adaptive system reconfiguration **Session Chair: Prof. ChiaHeng Tu** **Room: Conference Room 1 (101)**		
55	10:30-11:00	Using a Polymorphic VLIW Processor to Improve Schedulability and Performance for Mixed-Criticality Systems
		Joost Hoozemans, Jeroen van Straten, and Stephan Wong
33	11:00-11:30	Efficient and Balanced Charging of Reconfigurable Battery with Variable Power Supply
		Muhammad Shaheer, Nan Guan, Shuai Li, Q Wang, and Zili Shao
5	11:30-12:00	Online Energy-efficient Real-time Task Scheduling for Heterogeneous Multicore Systems
		Tien-Shun Yao, Ting-Hao Tsai, Ya-Shu Chen, Jing-Ho Chen, and Dai-Chang Chen
Session 6: Real-time scheduling **Session Chair: TBD** **Room: Conference Room 4 (106)**		
13	13:30-14:00	Online Admission of Non-Preemptive Aperiodic Mixed-Critical Tasks in Hierarchic Schedules
		Ali Syed, Daniel Gracia Pérez, and Gerhard Fohler

31	14:00-14:30	Worst-case Timing Analysis of Ring Networks with Cyclic Dependencies using Network Calculus
		Ahmed Amari and Ahlem Mifdaoui
17	14:30-15:00	Restart-Based Fault-Tolerance: System Design and Schedulability Analysis
		Fardin Abdi Taghi Abad, Renato Mancuso, Rohan Tabish, and Marco Caccamo

Short1(5): **Session Chair: Prof. Che-Wei Chang** **Room: Conference Room 1 (101)**		
50	13:30-13:48	Hybrid Self-Suspension Models in Real-Time Embedded Systems
		Georg von der Brüggen, Wen-Hung Huang, and Jian-Jia Chen
61	13:48-14:06	Artificial Skin for Human Prostheses, Enabled Through Wireless Sensor Networks
		Camilo Rojas and Jean-Dominique Decotignie
69	14:06-14:24	Towards the Design of Optimal Range Assignment for Elevator Groups under Fluctuant Traffic Loads
		Hailiang Dong, Edwin H.-M. Sha, Weiwen Jiang, Xianzhang Chen, Runyu Zhang, and Qingfeng Zhuge
66	14:24-14:42	A Survey of Energy-Efficient Task Synchronization for Real-Time Embedded Systems
		Jun Wu
58	14:42-15:00	Trading Utilization for Circuitry: Hardware-Software Co-design for Real-Time Software-Based Short-Circuit Protection
		Aaron Willcock and Nathan Fisher
Short2(5): **Session Chair: Prof. Duo Liu** **Room: Conference Room 1 (101)**		
18	13:30-13:48	An Adaptive Closed-Loop Approach for Timely Data Services
		Dinuni Fernando, Kyoung-Don Kang, and Yan Zhou
7	13:48-14:06	GPU Acceleration for Kernel Samepage Merging
		Wei-Cheng Lin, Chia-Heng Tu, Chih-Wei Yeh, and Shih-Hao Hung
41	14:06-14:24	Energy-Aware Page Replacement for NVM-based Hybrid Main Memory System
		Yiming Zhang, Jinyu Zhan, Junhuan Yang, Wei Jiang, Lin Li, and Li Yixin
67	14:24-14:42	Dynamic Module Partitioning for Library based Placement on Heterogeneous FPGAs
		Fubing Mao, Wei Zhang, Bingsheng He, and Siew-Kei Lam
73	14:42-15:00	FitCNN: A Cloud-Assisted Lightweight Convolutional Neural Network Framework for Mobile Devices
		Shiming Li, Duo Liu, Chaoneng Xiang, Jianfeng Liu, Yingjian Ling, Tianjun Liao, and Liang Liang

Poster Session: **Session Chairs: Prof. Pi-Cheng Hsiu and Prof. Chien-Chung Ho** **Room: Landis Inn Chuhu**	
21	Improving Core Allocation of Simulink Model for Embedded Multi-core Systems
	Sasuga Kojima, Masato Edahiro, and Takuya Azumi
27	Real-time Communication Analysis for SmartNoC
	Peng Chen, Weichen Liu, Lei Yang, Mengquan Li, and Nan Guan
68	A Half-Key Key Management Scheme with Honeycomb Deployment for Wireless Sensor Networks
	Yung-Feng Lu, Chin-Fu Kuo, and Bo-Kai Tseng
74	SDN-based Controller Switching for Resilience of Drones
	Young-Min Kwon and Kyung-Joon Park
75	Link Failover for Resilient Cyber-Physical Systems
	In-Hee Park and Kyung-Joon Park
76	If-conversion to reduce worst case execution time
	Soma Niloy Ghosh, Lava Bhargava, and Vineet Sahula
77	A dual shared stack for FSLM in Erika Enterprise
	Sri Muthu Narayanan Balasubramanian, Sara Afshar, Paolo Gai, Moris Behnam, and Reinder J. Bril
78	A Two Mode GC for Real-Time NAND Flash
	Tzu-Yen Chiu and Pei-Hsuan Tsai